What is claim d is:

1. A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a first electrode provided on the semiconductor substrate with the intervention of a gate insulation film;

a second electrode provided at least on the first electrode with the intervention of an intermediate insulation film; and

a pair of impurity regions of a second conductivity type provided in a spaced relation in the semiconductor substrate, at least one of the impurity regions comprising a low concentration impurity region, an intermediate concentration impurity region and a high concentration impurity region sequentially arranged in this order from a region located underneath the first electrode.

2. A semiconductor device as set forth in claim 1, further comprising conductive layers respectively provided on at least one of the first electrode and the second electrode, and on the high concentration impurity region.

3. A semiconductor device as set forth in claim 2, wherein the conductive layers is silicide films.

4. A semiconductor device as set forth in claim 1, further comprising sidewall insulation films provided on at least one of the side walls of the first electrode and the second electrode.

5. A semiconductor device as set forth in claim 1, wherein the pair of impurity regions of the second conductivity type each

include the low concentration impurity region, the intermediate concentration impurity region and the high concentration impurity region sequentially arranged in this order from the region located underneath the first electrode.

6. A semiconductor device as set forth in claim 1, wherein the intermediate concentration impurity region is provided only in a surface portion of the semiconductor substrate, or extend from the surface portion of the semiconductor substrate to the inside of the substrate as surrounding the high concentration impurity region, or as being partly or entirely surrounded by the low concentration impurity region.

7. A semiconductor device as set forth in claim 1, wherein the high concentration impurity region is provided as being surrounded by the low concentration impurity region and the intermediate concentration impurity region, or surrounded only by the low concentration impurity region.

8. A semiconductor device as set forth in claim 1, wherein the low concentration impurity region has an impurity concentration on the order of 10^{18} ions/cm^3, the intermediate concentration impurity region has an impurity concentration on the order of 1×10^{18} to 10^{19} ions/cm^3, and the high concentration impurity region has an impurity concentration on the order of 1×10^{20} to 10^{21} ions/cm^3.

9. A semiconductor device as set forth in claim 1, wherein the

low concentration impurity region is disposed at a depth of 100 to 600 nm, the intermediate concentration impurity is disposed at a depth of about 100 to about 600 nm, and the high concentration impurity region is disposed at a depth of about 100 to about 400 nm as measured from the surface of the semiconductor substrate.

10. A semiconductor device as set forth in claim 1, wherein the first electrode has a greater thickness than the second electrode.

11. A semiconductor device as set forth in claim 1, wherein the second electrode entirely covers the first electrode and further extends to one side or opposite sides of the first electrode on the semiconductor substrate, or disposed only on the first electrode having a smaller size than the first electrode.

12. A semiconductor device as set forth in claim 1, wherein the first electrode and the second electrode serve as a floating gate electrode and a control gate electrode, respectively, of a memory transistor.

13. A process for fabricating a semiconductor device, comprising the steps of:

(i) forming a gate insulation film on a semiconductor substrate of a first conductivity type and forming a first electrode on the gate insulation film;

(ii) subjecting the resulting substrate to implantation of ions of a second conductivity type by using the first electrode as a mask;

(iii) forming an intermediate insulation film on the resulting semiconductor substrate and forming a second electrode on the intermediate insulation film with at least a part of the second electrode being disposed on the first electrode;

(iv) subjecting the resulting substrate to implantation of ions of the second conductivity type with an implantation energy that causes the ions to be implanted into a region of the semiconductor substrate formed with either of the first and second electrodes but forbids the ions to be implanted into a region of the semiconductor substrate formed with the first and second electrodes in a stacked relation; and

(v) subjecting the resulting substrate to implantation of ions of the second conductivity type with an implantation energy that forbids the ions to penetrate through the first electrode and the second electrode;

whereby the semiconductor device is fabricated as having at least one impurity region of the second conductivity type including a low concentration impurity region, an intermediate concentration impurity region and a high concentration impurity region sequentially arranged in this order from a region located underneath the first electrode.

14. A process as set forth in claim 13, further comprising the step of forming sidewall insulation films on side walls of at least one of the first electrode and the second electrode between the steps (iv) and (v), wherein the implantation energy to be employed for the implantation of the ions of the second conductivity type in the step (v) is at a level that forbids the ions to penetrate through

the sidewall insulation films.

15. A process as set forth in claim 13, further comprising the steps of: forming sidewall insulation films on side walls of at least one of the first electrode and the second electrode between the steps (iv) and (v); and forming conductive layers on at least one of the first electrode and the second electrode and on the high concentration impurity region through a salicide process employing a high melting point metal film after the step (v).

16. A process as set forth in claim 13, wherein the second electrode has a smaller thickness than the first electrode.

17. A process as set forth in claim 13, wherein the second electrode is formed as entirely covering the first electrode and further extending to one side or opposite sides of the first electrode on the semiconductor substrate, or disposing only on the first electrode having a smaller size than the first electrode.